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PowerPC™

Errata to **MPC750 RISC Microprocessor User's Manual**

This errata describes corrections to the *MPC750 RISC Microprocessor User's Manual*. These corrections also apply to the MPC740, which is described in *MPC750 RISC Microprocessor User's Manual*. For convenience, the section number and page number of the errata item in the user's manual are provided.

To locate any published updates for this document, refer to the world-wide web at http://www.mot.com/powerpc.

Section/Page	Changes
2.1.1, 2-7	The implementation note for the decrementer register (DEC) should read as follows: In the MPC750 the decrementer register is decremented and the time base is incremented at a speed that is one-fourth the speed of the bus clock.
2.1.2.2, 2-12	In Table 2-4, replace the description of HID0[DBP] (bit 1), with the following:

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1	DBP	Disable 60x bus address and data parity generation. 0 The system generates address and data parity. 1 Parity generation is disabled and parity signals are driven to 0 during bus operations. When parity generation is disabled, all parity checking should also be disabled and parity signals need not be connected.

Replace the description of HID0[BTIC] (bit 26), with the following:

26	BTIC	BTIC enable. Used to enable use of the 64-entry branch instruction cache. 0 The BTIC contents are invalidated and the BTIC behaves as if it were empty. New entries cannot be added until the BTIC is enabled. 1 The BTIC is enabled and new entries can be added.

2.1.2.4.5, 2-18 Replace Table 2-11 with the following:

Table 2-11. PMC2 Events—MMCR0[26–31] Select Encodings

Encoding	Description
00 0000	Register holds current value.
00 0001	Counts processor cycles.
00 0010	Counts completed instructions. Does not include folded branches.
00 0011	Counts transitions from 0 to 1 of TBL bits specified through MMRC0[RTCSELECT]. 00 = 47, 01 = 51, 10 = 55, 11 = 63.
00 0100	Counts instructions dispatched. 0, 1, or 2 instructions per cycle.
00 0101	Counts L1 instruction cache misses.
00 0110	Counts ITLB misses.
00 0111	Counts L2 instruction misses.
00 1000	Counts branches predicted or resolved not taken.
00 1001	Counts MSR[PR] bit toggles.
00 1010	Counts times reserved load operations completed.
00 1011	Counts completed load and store instructions.
00 1100	Counts snoops to the L1 and the L2.
00 1101	Counts L1 cast-outs to the L2.
00 1110	Counts completed system unit instructions.
00 1111	Counts instruction fetch misses in the L1.
01 0000	Counts branches allowing out-of-order execution that resolved correctly.
All others	Reserved.

4.5.11, 4-20 Remove Table 4-10, “Trace Exception—SRR1 Settings.” This interrupt is implemented as defined by the OEA. Remove the Table 4-10 and the introductory text.

5.1.7, 5-18 Table 5-4, delete the second row in table (**lwarx** or **stwcx.** with W = 1).

7.2.5.2.1, 7-14 For $\overline{\text{ARTRY}}$, change "Timing Comments," "Negation," first paragraph, last sentence to the following:

First the buffer goes to high impedance for a minimum of one-half processor cycle (dependent on the clock mode), then it is driven negated for one-half bus cycle before returning to high impedance.

9.1.2, 9-5 In Table 9-1, replace the description of L2CR[L2DO] (bit 9), with the following:

9	L2DO	L2 data-only. Setting this bit inhibits the caching of instructions in the L2 cache. All accesses from the L1 instruction cache are treated as cache-inhibited by the L2 cache (bypass L2 cache, no L2 tag look-up performed).

11.2.1.5, 11-7 Replace Table 11-6 with the following:

Table 11-16. PMC2 Events—MMCR0[26–31] Select Encodings

Encoding	Description
00 0000	Register holds current value.
00 0001	Counts processor cycles.
00 0010	Counts completed instructions. Does not include folded branches.
00 0011	Counts transitions from 0 to 1 of TBL bits specified through MMRC0[RTCSELECT]. 00 = 47, 01 = 51, 10 = 55, 11 = 63.
00 0100	Counts instructions dispatched. 0, 1, or 2 instructions per cycle.
00 0101	Counts L1 instruction cache misses.
00 0110	Counts ITLB misses.
00 0111	Counts L2 instruction misses.
00 1000	Counts branches predicted or resolved not taken.
00 1001	Counts MSR[PR] bit toggles.
00 1010	Counts times reserved load operations completed.
00 1011	Counts completed load and store instructions.
00 1100	Counts snoops to the L1 and the L2.
00 1101	Counts L1 cast-outs to the L2.
00 1110	Counts completed system unit instructions.
00 1111	Counts instruction fetch misses in the L1.
01 0000	Counts branches allowing out-of-order execution that resolved correctly.
All others	Reserved.

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